Electronic Version
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# Claims

[c1] A method of operating a programmable logic integrated circuit comprising:
after providing power to the integrated circuit, in a first state, reading a first pattern stored at a first address from a nonvolatile configuration memory of the programmable logic integrated circuit;
following the first state, in a second state, comparing the first pattern to an expected first pattern and returning to the first state if the first pattern does not match the expected first pattern;
if the first pattern matches the expected first pattern, continuing to a third state, reading a second pattern stored at a second address from the nonvolatile configuration memory of the programmable logic integrated circuit; and
following the third state, in a fourth state, comparing the second pattern to an expected second pattern and returning to the first state if the second pattern does not match the expected second pattern.

[c2] The method of claim 1 further comprising:
if the second pattern matches the expected second pat-

tern, continuing to a fifth state, reading a third pattern stored at a third address from the nonvolatile configuration memory of the programmable logic integrated circuit; and

following the fifth state, in a sixth state, comparing the third pattern to an expected third pattern and returning to the first state if the third pattern does not match the expected third pattern.

[c3] The method of claim 2 further comprising:

if the third pattern matches the expected third pattern, continuing to a seventh state, reading a fourth pattern stored at a fourth address from the nonvolatile configuration memory of the programmable logic integrated circuit; and

following the fifth state, in a sixth state, comparing the fourth pattern to an expected fourth pattern and returning to the first state if the fourth pattern does not match the expected fourth pattern.

[c4] The method of claim 3 further comprising:

if the fourth pattern matches the expected fourth pattern, permitting configuration of a programmable logic core of the programmable logic integrated circuit using configuration data stored in the nonvolatile configuration memory.

[c5] The method of claim 1 wherein the expected first pattern comprises all 0s and the expected second pattern comprises all 1s.

[c6] The method of claim 2 wherein the expected third pattern comprises alternating 0s and 1s.

[c7] The method of claim 3 wherein the expected fourth pattern comprises alternating 0s and 1s.

[c8] The method of claim 1 further comprising:
when erasing the nonvolatile configuration memory, preserving the first pattern stored at the first address and the second pattern stored at the second address.

[c9] The method of claim 1 further comprising:
when configuring the configuration memory, programming the expected first pattern at the first address and the expected second pattern at the second address.

[c10] A method of operating a programmable logic integrated circuit comprising:
after providing power to the integrated circuit, starting a timer circuit to provide a time count value;
in a first state, reading a first pattern stored at a first address from a nonvolatile configuration memory of the programmable logic integrated circuit;
if the time count value is a max count value, disabling

transfer of configuration data from the nonvolatile configuration memory to the programmable logic core;
if the time count value is not the max count value, in a second state, comparing the first pattern to an expected first pattern and returning to the first state if the first pattern does not match the expected first pattern;
if the first pattern matches the expected first pattern, continuing to a third state, reading a second pattern stored at a second address from the nonvolatile configuration memory of the programmable logic integrated circuit; and
following the third state, in a fourth state, comparing the second pattern to an expected second pattern and returning to the first state if the second pattern does not match the expected second pattern.

[c11] The method of claim 10 further comprising:
if the second pattern matches the expected second pattern, continuing to a fifth state, reading a third pattern stored at a third address from the nonvolatile configuration memory of the programmable logic integrated circuit;
following the fifth state, in a sixth state, comparing the third pattern to an expected third pattern and returning to the first state if the third pattern does not match the expected third pattern;

if the third pattern matches the expected third pattern, continuing to a seventh state, reading a fourth pattern stored at a fourth address from the nonvolatile configuration memory of the programmable logic integrated circuit; and

following the fifth state, in a sixth state, comparing the fourth pattern to an expected fourth pattern and returning to the first state if the fourth pattern does not match the expected fourth pattern.

[c12] A programmable logic integrated circuit comprising:

a nonvolatile configuration memory comprising configuration data and at least two test patterns;

a programmable logic core, coupled to the nonvolatile configuration memory and comprising volatile memory, configured using configuration data stored in the configuration memory upon power up of the programmable logic integrated circuit;

a controller circuit coupled to the nonvolatile configuration memory, comprising circuitry to inhibit configuration of the programmable logic core until the at least two test patterns stored in the nonvolatile configuration memory are read correctly.

[c13] The programmable logic integrated circuit of claim 13 further comprising:

a power-on reset circuit to provide a power-on reset

signal to the controller circuit upon power up of the programmable logic integrated circuit, wherein the controller circuit begins operation after receiving the power-on reset signal.

[c14] The programmable logic integrated circuit of claim 12 wherein the nonvolatile configuration memory comprises at least four test patterns, and the controller circuit inhibits configuration of the programmable logic core until the at least four patterns stored in the nonvolatile configuration memory are read correctly.

[c15] The programmable logic integrated circuit of claim 12 wherein a first test pattern is stored at a first address, the first test pattern comprises 0s, a second test pattern is stored at a first address, the second test pattern comprises 1s.

[c16] The programmable logic integrated circuit of claim 14 further comprising:
a power-on reset circuit coupled to a VCC pin of the programmable logic integrated circuit and providing a power-on reset signal to the controller circuit.

[c17] A programmable logic integrated circuit comprising:
a configuration memory comprising configuration data stored in nonvolatile memory cells;

a plurality of first sense amplifier circuits coupled to the configuration memory;
a first verification sense amplifier circuit coupled to the configuration memory;
a programmable logic core, configurable to perform user functions, coupled to the plurality of first sense amplifier circuits, wherein the configuration data is used to configure the programmable logic core; and
a controller circuit coupled to the first verification sense amplifier circuit and at least one address line of a plurality of an address lines provided to the configuration memory.

[c18] The programmable logic integrated circuit of claim 17 further comprising:
a second verification sense amplifier circuit coupled between the configuration memory and the controller circuit.

[c19] The programmable logic integrated circuit of claim 17 wherein when an output of the first sense amplifier is a 0 and the at least one address line comprises a 1 signal, the controller circuit generates a signal indicative of an error condition.

[c20] The programmable logic integrated circuit of claim 19 wherein when an output of the first sense amplifier is a 1

and the at least one address line comprises a 1 signal, the controller circuit generates a signal indicative of an nonerror condition.

[c21] The programmable logic integrated circuit of claim 18 wherein when an output of the first sense amplifier is a 1, an output of the second sense amplifier is a 0, and the at least one address line comprises a 1 signal, the controller circuit generates a signal indicative of an nonerror condition.

[c22] The programmable logic integrated circuit of claim 21 wherein when an output of the first sense amplifier is a 0, an output of the second sense amplifier is a 1, and the at least one address line comprises a 0 signal, the controller circuit generates a signal indicative of an nonerror condition.

[c23] The programmable logic integrated circuit of claim 17 wherein there are at least 64 first sense amplifier circuits.

[c24] A method of operating a programmable logic integrated circuit comprising:
programming a nonvolatile configuration memory of the programmable logic integrated circuit with a user's configuration data;

programming at least two additional bits of each word of the configuration memory where the user's configuration data is stored with bits depending on an address of the word.

[c25] The method of claim 24 wherein when the address is even, the two additional bits are 10, and when the address is odd, the two additional bits are 01.

[c26] The method of claim 24 wherein when the address is even, the two additional bits are 01, and when the address is odd, the two additional bits are 10.

[c27] The method of claim 24 further comprising:
transferring in parallel the user's configuration data from the configuration memory to a programmable logic core of the programmable logic integrated circuit;
verifying the transfer in parallel of the user's configuration data by reading and comparing the two additional bits to expected results for the two additional bits;
restarting transferring in parallel of the user's configuration data if the two additional bits do not match the expected results for the two additional bits.

[c28] A method of operating a programmable logic integrated circuit comprising:
transferring in parallel a user's configuration data stored

in a configuration memory to a programmable logic core of the programmable logic integrated circuit;
verifying the transfer of the user's configuration data by reading and comparing at least two additional bits of each word of the parallel transfer to expected results for these two additional bits;
restarting the transfer of the user's configuration data if the at least two additional bits do not match the expected results for the two additional bits.

[c29] The method of claim 28 wherein the user's configuration data is transferred 64 bits in parallel.

[c30] The method of claim 28 further comprising:
permitting configuration of the programmable logic core when the two additional bits match the expected results for the two additional bits.

[c31] A method of operating a programmable logic integrated circuit comprising:
after providing power to the integrated circuit, in a first state, reading a first pattern stored at a first address from a nonvolatile configuration memory of the programmable logic integrated circuit;
following the first state, in a second state, comparing the first pattern to an expected first pattern and returning to the first state if the first pattern does not match the ex-

pected first pattern;

if the first pattern matches the expected first pattern, continuing to a third state, reading a second pattern stored at a second address from the nonvolatile configuration memory of the programmable logic integrated circuit;

following the third state, in a fourth state, comparing the second pattern to an expected second pattern and returning to the first state if the second pattern does not match the expected second pattern;

if the second pattern matches the expected second pattern, permitting configuration of a programmable logic core of the programmable logic integrated circuit using configuration data stored in the nonvolatile configuration memory;

transferring in parallel a user's configuration data stored in the configuration memory to the programmable logic core of the programmable logic integrated circuit;

verifying the transfer of the user's configuration data by reading and comparing at least two additional bits of each word of the parallel transfer to expected results for these two additional bits; and

restarting the transfer of the user's configuration data if the at least two additional bits do not match the expected results for the two additional bits.

[c32] The method of claim 31 wherein when an address of a row where the user's configuration is stored is even, the two additional bits are 10, and when the address is odd, the two additional bits are 01.

[c33] The programmable logic integrated circuit of claim 31 wherein when an address of a row where the user's configuration is stored is even, the two additional bits are 01, and when the address is odd, the two additional bits are 10.